Refine Search

Search Results -

Terms	Documents
L30 same synchronous	4

Database: US Pre-Grant Publication Full-Text Database; US Patents Full-Text Database; US OCR Full-Text Database; EPO Abstracts Database; JPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L33

Refine Search | Recall Text | Clear | Interrupt

Search History

DATE: Thursday, December 22, 2005 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L33	L30 same synchronous	4	L33
L32	L30 same synchroneous	0	L32
L31	L30 same shift$	0	L31
L30	interlocked near3 pipeline	59	L30
L29	L1 same shift$	2	L29
L28	L26 and l23	6	L28
L27	L26 same l23	0	L27
L26	manipulating adj1 data	2674	L26
L25	L24 same controller	3	L25
L24	L23 same (array or matrix)	56	L24
L23	L20 same scan	356	L23
L22	scan adj1 circuit$	3432	L22
L21	L20 same cascaded	28	L21
L20	L9 same shift$	4651	L20

L19	L18 same l17	1	L19
L18	scan adj1 controller	1007	L18
L17	process adj1 controller	8477	L17
L16	L15 same l9	2	L16
L15	clock adj1 shifter	32	L15
L14	L13 same scan	11	L14
L13	L12 same controller	46	L13
L12	L10 same shift$ same clock	428	L12
L11	L10 same cascaded same shift$	5	L11
L10	L9 same (l1 or latch)	4907	L10
L9	(valid or invalid) same (data or datum)	67978	L9
L8	L7 same controller	6	L8
L7	cascaded near3 (l1 or latch)	293	L7
L6	l1 same matrix	2	L6
L5	L4 same l3 same matrix	1	L5
L4	scan adj1 data	8819	L4
L3	process adj1 data	53105	L3
L2	L1 adj1 array	1	L2
L1	state adj1 holding adj1 element	50	L1

END OF SEARCH HISTORY

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#
Generate Collection Print

L6: Entry 1 of 2 File: USPT Dec 4, 2001

DOCUMENT-IDENTIFIER: US 6327071 B1
TITLE: Drive methods of array-type light modulation element and flat-panel display

Detailed Description Text (47):
After reset scan of each light modulation element, write scan for selecting the displacement operation or state holding of the element is executed, whereby the state before the write scan is prevented from affecting the next operation because of the hysteresis characteristic of the element, and stable write scan can be executed. It is made possible to drive the two-dimensional light modulation array of the simple matrix structure without contradiction, namely, so as to reliably hold the on/off state of each pixel on the nonselection scan line set at the write scan time because of the hysteresis characteristic of the element.

Previous Doc Next Doc Go to Doc#

L16: Entry 1 of 2 File: USPT Apr 11, 2000

DOCUMENT-IDENTIFIER: US 6049488 A
TITLE: Clock synchronous semiconductor memory device capable of preventing outputting of invalid data

Detailed Description Text (61):
When internal clock signal intCLK rises to H-level, half-clock shifter 1eb takes in output signal OEMFS2D of half-clock shifter 1ea, and lowers output enable signal OEM to L-level. Therefore, output buffer circuit 910b attains the output high-impedance state. Upon this deactivation of output enable signal OEM, internal data DD is continuously applied from gate circuit 910a during this clock cycle #2. Therefore, a sufficiently long hold time tH can be ensured, and output of invalid data does not occur.

Detailed Description Text (66):
Thereafter, output enable signal OEM is activated so that setup time tS of internal data DD with respect to output enable signal OEM can be sufficiently increased. Invalid data is not output even at the time of transition from the data output masked state to the data output state, and output data Dout can be stably produced in accordance with internal read data RD. Particularly, if the delay time of half-clock shifter 1eb is much longer than the delay time of gate circuit 910a, setup time tS can be made sufficiently long.

Detailed Description Text (68):
In clock cycle #5, half-clock shifter 1eb takes in signal OEMFS2D at L-level, and drives output enable signal OEM to L-level in synchronization with the rising of internal clock signal intCLK. Thereby, output circuit 910 attains the output high-impedance state. In this state, gate circuit 910a is in the latching state (internal clock signal CLKO maintains L-level because signal OEMFS2D is at L-level), and the hold time of data DD with respect to the falling of output enable signal OEM is sufficiently long. Therefore, invalid data is not output at the time of transition to this output high-impedance state.

Detailed Description Text (75):
In the structure shown in FIG. 12, when signal OEMD from half-clock shifter 1ec is at L-level inactive, internal clock signal CLKO for data output is at H-level, and gate circuit 910a transmits internal read data RD to output buffer circuit 910. Therefore, internal read data RD is transmitted to output buffer circuit 910b before output enable signal OEM is activated, so that the set up time of internal data DD with respect to output enable signal OEM can be made long. When signal OEMFSD attains the inactive state of L-level and signal OEMD is at H-level or active, internal clock signal CLKO for data output attains L-level, and gate circuit 910a is turned off and attains the state of latching the applied date. Therefore, gate circuit 910a attains the latching state before deactivation of output enable signal OEM, and the hold time of internal data DD with respect to output enable signal OEM can be increased. Thereby, output of invalid data can be prevented. Operation of the data output control circuit and the output circuit shown in FIG. 12 will be described below with reference to a timing chart of FIG. 13.

Detailed Description Text (78):

In clock cycle #1, half-clock shifter 1eb takes in applied signal OEMFSD in synchronization with internal clock signal intCLK, and drives output enable signal OEM to H-level. Thereby, output buffer circuit 910b attains the output low-impedance state, and buffers internal data DD to produce output data Dout. When output buffer circuit 910b attains the operating state, i.e., when output enable signal OEM is activated to attain H-level, internal data DD is already transmitted so that setup time tS of internal data DD with respect to output enable signal OEM has a sufficient length. Therefore, output data Dout is produced in accordance with internal data DD without producing invalid data.

Detailed Description Text (82):
Internal clock signal CLKO for output is held at L-level until half-clock shifter 1ec takes in output enable signal OEM and drives signal OEMD to L-level in synchronization with the falling of internal clock signal intCLK in clock cycle #5. Therefore, internal data DD at the time of deactivation of output enable signal OEM has hold time tH equal to half the clock cycle of internal clock signal intCLK with respect to output enable signal OEM, and output of invalid data can be reliably prevented at the time of deactivation of output enable signal OEM. Thereafter, output buffer circuit 910b holds the output high-impedance state as a result of deactivation of output enable signal OEM, although internal clock signal CLKO is held at H-level and gate circuit 910a is held ON.

Detailed Description Text (90):
Meanwhile, half-clock shifter 1eb takes in signal OEMFS2D at H-level in synchronization with the rising of internal clock signal intCLK in clock cycle #1, and drives output enable signal OEM to H-level. At this time, internal read data RD has been transmitted to output buffer circuit 910b through on-state gate circuit 910a, and output buffer circuit 910b buffers internal data DD in accordance with active output enable signal OEM to produce output data Dout. In this case, therefore, setup time tS of internal data DD is sufficiently long, similarly to the foregoing embodiment 3, and output data Dout is produced without being accompanied by invalid data.

Detailed Description Text (93):
In clock cycle #2, half-clock shifter 1eb likewise takes in signal OEMFS2D at L-level in synchronization with the rising of internal clock signal intCLK so that output enable signal OEM is driven to L-level, and output buffer circuit 910b attains the output high-impedance state. In this clock cycle #2, internal clock signal CLKO for output is fixed at L-level while internal clock signal intCLK is at H-level, and therefore gate circuit 910a is in the latching state. Subsequently, signal OEMD from half-clock shifter 1ec falls to L-level in synchronization with the falling of internal clock signal intCLK, and internal clock signal CLKO attains H-level. When output enable signal OEM changes to the inactive state of L-level in clock cycle #2, internal data DD is therefore in the latched state for a period equal to half the clock cycle of internal clock signal intCLK. Accordingly, internal data DD has sufficiently long hold time tH with respect to output enable signal OEM. Consequently, it is possible to prevent output of invalid data at the time of transition to the masked state.

Detailed Description Text (95):
In clock cycle #3, half-clock shifter 1eb takes in signal OEMFS2D at H-level in synchronization with the rising of internal clock signal intCLK so that output enable signal OEM rises to H-level, and signal OEMD from half-clock shifter 1ec subsequently rises to H-level in synchronization with the falling of internal clock signal intCLK. At the time of transition of output enable signal OEM to the active state, therefore, internal read data RD(2) is already transmitted, as data DD(2), to output buffer circuit 910b so that setup time tS is sufficiently long. Therefore, internal data DD(2) is buffered without being accompanied by invalid data, and output data Dout(2) is output.

Detailed Description Text (97):
In clock cycle #5, half-clock shifter 1eb takes in signal OEMFS2D at L-level in synchronization with the rising of internal clock signal intCLK, and lowers output enable signal OEM to L-level. At this time, internal clock signal CLKO is still at L-level, and gate circuit 910a is in the latching state. When internal clock signal intCLK falls to L-level, half-clock shifter 1ec takes in output enable signal OEM at L-level, and drives its output signal OEMD to L-level. Thereby, internal clock signal CLKO for output is fixed to H-level. At the time of transition of output enable signal OEM to the inactive state, therefore, internal read data DD is in the latched state for a period equal to half the clock cycle so that hold time tH is sufficiently long, and output of invalid data is prevented.

Detailed Description Text (111):
In synchronization with the falling of internal clock signal intCLK in clock cycle #2, output signal DQMD of half-clock shifter 1jc rises to H-level. Thereby, the output signal of inverter 1y attains L-level, and output signal CLKO of NAND circuit 1kb attains H-level so that gate circuit 910a is turned on, and read data RD is transmitted to output buffer 910b. At this time, however, signal DQMi from half-clock shifter 1jb rises to H-level, and complementary mask signal /DMQi attains L-level in synchronization with the rising of internal clock signal intCLK. Therefore, output buffer circuit 910b attains the output high-impedance state so that this invalid data DD(1) is not output.

Detailed Description Text (112):
In clock cycle #3, signal DQMi from half-clock shifter 1jb falls to L-level, and complementary internal mask signal /DQMi attains H-level in synchronization with the rising of internal clock signal intCLK so that output buffer circuit 910b attains the output low-impedance state again. At this time, internal clock signal CLKO is already at H-level attained according to signal DQMD and in synchronization with the falling of internal clock signal intCLK in clock cycle #2, and this H-level state is maintained until falling of internal clock signal intCLK in clock cycle #3. Therefore, internal read data RD is already transmitted to output buffer circuit 910b before falling of signal DQMi. Accordingly, a sufficiently long setup time is kept, and valid data is output without outputting invalid data.

Detailed Description Text (125):
In clock cycle #2, internal data output mask instruction DQMi attains H-level in synchronization with the rising of internal clock signal intCLK, and output buffer circuit 910b attains the output high-impedance state. In this state, internal clock signal CLKO for output holds L-level, and therefore gate circuit 910a holds the latching state so that hold time tH of internal data DD at the time of transition of output buffer circuit 910b to the output high-impedance state is equal to one clock cycle period and is sufficiently long, resulting in prevention of output of invalid data. In clock cycle #2, output signal DQM0D of half-clock shifter 1ja attains L-level in synchronization with the falling of internal clock signal intCLK so that control logic gate 1m produces internal clock signals CLKO and /CLKO in accordance with internal clock signal intCLK.

Detailed Description Text (129):
Setup time tS of internal data DD with respect to output enable signal OEM can be sufficiently increased by setting the delay time of one-clock shifter 1e (gate delay of the counter) to be longer the delay time of control logic gate 1m and the delay time of gate circuit 910a. However, this arrangement would reduce hold time tH of internal data DD at the time of transition of output enable signal OEM to the inactive state, and therefore invalid data may be output together with output data Dout1 in FIG. 19 at the time of transition to the output high-impedance state. Meanwhile, if setup time tS is reduced, hold time tH increases, and invalid data is not output at the time of transition of output enable signal OEM to the inactive state. However, reduced setup time tS may cause output of invalid data as can be seen from data Dout2 in FIG. 19. For preventing this, internal read data RD' is

held in the latched state when the last data in the burst length is output. In this case, sufficiently long setup time tS may be employed. In other words, such a structure may be employed that internal clock signal CLKO for data output rises to H-level at a fast timing relative to activation of output enable signal OEM, to make conductive gate circuit 910a. Since hold time tH is sufficiently long, invalid data is not output according to this structure as can be seen from internal data DD' and output data Dout1'. For internal data DD', internal clock signal CLKO is produced, and latched read data RD'(3) is repetitively applied. Thus, the same data is continuously applied as internal data DD' so that hold time tH can be increased.

Previous Doc Next Doc Go to Doc#